





NanoTech Poland 2023 13th International Conference 14 - 16 June 2023, Poznań, Poland



Advanced substrates for measurements of nanomaterials

Bartosz Cz. Pruchnik^a, Janusz D. Fidelus^b, Krzysztof Kwoka^a, Andrzej Sierakowski^c, Teodor P. Gotszalk^a ^a Department of Nanometrology, Wrocław University of Science and Technology, Janiszewskiego 11/17, 50-370, Wrocław, Poland ^b Time and Length Department, Central Office of Measures, Elektoralna 2, 00-139, Warsaw, Poland ^c Łukasiewicz Research Network, Institute of Microelectronics and Photonics, Lotników 32/46, Warsaw 02-668, Poland



The dimensions of nanoparticles render them comparable to the surface details of many available substrates. Repeatable measurement of nanoparticles requires a stable, reliable substrate that does not interfere with the measurement of the specimen in any quantity [1]. For topography, that would be realized by surface roughness appropriately smaller than nanoparticle dimensions, etc. The realization of substrates has to simultaneously allow for measurement with microscopic tools and therefore enlarge the contact area of nanoparticles.



We present a series of substrates with surface features prepared specifically for the measurement of nanowires (NWs). Features characterize an elevation of about 500 nm above the substrate, an electrical resistivity of $11 \cdot 10^{-8} \mu \Omega$, and a thermal conductivity of $1,6 \cdot 10^{3}$ W/K. Details allow for direct placement of NWs, electrical connection, and measurement of a given quantity. They are prepared in a more condensed, less accessible form, which has to be accessed with nanomanipulators (e.g., Kleindiek MM3A-EM) or more loosely with electrical connections leading out of the sample, allowing for measurement of mechano-electro-thermal properties.

NANOPARTICLES INTEGRATION

Transfer to desired location

Bonding with material deposited with focused electron beam

> Novel devices

development





Figure 2. The process of transferring and mounting nanowires onto a substrate. Visible transport of the nanowire with manipulator and focused electron beam-induced deposition (FEBID) deposited mounting pads





Figure 1. Different substrates with orientation patterns and various openings

SUBSTRATES FOR IMPROVED CURRENT MEASUREMENTS

NXXXX

➢ Fine details for nanowires placement ► Metal over oxide on silicon ➢Gaps as narrow as 500 nm Substrates 10 by 10 fields of 12 by 12 structures



Figure 3. Substrates for measurement of nanoparticles: matrix of separated electrically and thermally islands for measurement of nanoparticles imaged with optical microscope

TWO-POINT RESISTANCE MEASUREMENT

> Nanowire deposited between two contacted metal pads > Contacting with nanomanipulators or measurement probes Still imperfect wire-substrate interface





Figure 4. Realisation of the two-point resistance measurement

FOUR-POINT RESISTANCE MEASUREMENT



Why four point?

Irrelevant probe and contacts resistance ► Hardly realised by SPM

Allows for mechanoelectrical measurements



Vacuum Nanoelectronics Conferenc IVNC) 2017

Figure 5. Single section of electrically connected setup with nanowire placed imaged with scanning electron microscope.

SUMMARY

ACKNOWLEDGMENTS

- A new line of substrates for NW will allow for correlative microscopy of their thermal, mechanical, and electrical properties.
- Simultaneous measurement of various phenomena is a necessity in determining transducing properties such as thermoelectricity, piezoelectricity, or thermal expansion.
- In further development, substrates will incorporate active structures, enabling the determination of even more parameters.

The following research has been conducted with financing from the project 19ENG05 – NanoWires funded from the EMPIR programme (European Union's Horizon 2020).



research and innovation programme and the EMPIR Participating States



https://www.ptb.de/empir2020/nanowires/home/

REFERENCES

[1.] Wielgoszewski, G., Jóźwiak, G., Babij, M., Baraniecki, T., Geer, R., & Gotszalk, T. (2014). Investigation of thermal effects in through-silicon vias using scanning thermal microscopy. Micron, 66, 63-68.